IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Kiran V. Chatty et al.	Confirmation No.: 5747
Appln. No.	: 10/711,748	Group Art Unit: 2836
Filed	: 10/01/2004	Examiner: Z. Kitov
For	: HIGH VOLTAGE ESD POWER CLAMP	

RESPONSE UNDER 37 C.F.R. § 1.111

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria, VA 22314

Sir:

Responsive to the Office Action of February 28, 2006, the period for response extending until May 30, 2006 (May 28, 2006 being a Sunday and May 29, 2006 being a U.S. Federal holiday), reconsideration of this action and allowance of all the claims of the present application are respectfully requested and are now believed appropriate in view of the following amendments and remarks.

Amendments to the Specification begin on page 3 of this paper;

Amendments to the Claims are reflected in the listing of claims which begins on page 4;

Amendments to the Drawings begin on page 9 of this paper and include both an attached replacement sheet and an annotated sheet showing changes.

Remarks begin on page 10 of this paper.

An Appendix including the New Sheet of drawings is attached following this paper.

Applicants believe no fees are required at this time. However, if any fees are deemed necessary for consideration of this amendment, including any fees for extensions of time, which are hereby petitioned under 37 C.F.R. §1.136(a), such fees are hereby authorized to be charged to **Deposit Account No. 09-0456** (Burlington).

AMENDMENTS TO THE SPECIFICATION

Please enter new paragraph [0019.1] after paragraph [0019] as follows:

[0019.1] Figure 3a illustrates an alternative embodiment of the invention depicted in Figure 3;

Please replace paragraph [0040] with the following amended paragraph:

[0040] It should be noted that although nFETs and pFETs are used in the above examples, any type of appropriate semiconductor device may be used in embodiments of the power clamp circuit and remain within the scope of the invention. It should also be noted that in FIGS. 3 and 4, although a single inverter network is shown, any suitable number of network inverters may be incorporated into the circuit to allow the power clamp to work at any desired voltage. Incorporating additional inverters into the circuit may also require additional corresponding capacitors, and/or resistors in the RC-trigger network as should be understood by those of ordinary skill in the art. Additionally, in FIGS. 3 and 4, any number of transistor-like devices may be used in connection with the first and second nFETs 32 and 30 in order to allow the power clamp to function in virtually in any voltage environment, and corresponding additions to the resistive network to bias the additional nFETs, *see, e.g.*, transistor Tn and resistor Rn depicted in FIG. 3a. Although nFETs and pFETs are used for illustration purpose, any type of switching device suitable to the task may be used for the operation of the power clamp.

AMENDMENT TO THE CLAIMS

This listing of claims is a copy of all pending claims, which identifies the status of each claims, and which replaces all prior versions, and listing of claims in the application.

Listing of Claims

1. (Currently amended) A power clamp for an integrated circuit, comprising:

a transistor network composed of a first and second transistor respectively connected between a voltage source and a ground;

a bias network configured to bias a gate of a the first transistor of the transistor network to a portion of a voltage value of the voltage source; and

a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a the second transistor of the transistor network.

2. (Original) The power clamp of claim 1, wherein the transistor network comprises a first nFET and a second nFET connected in series with one another between the voltage source and a ground.

3. (Original) The power clamp of claim 2, wherein the transistor network further comprises a third nFET connected in series with the first nFET and the second nFET between the voltage source and the ground.

4. (Previously presented) A power clamp for an integrated circuit, comprising:

a transistor network connected between a voltage source and a ground;

a bias network configured to bias a gate of a first transistor of the transistor network to a portion of a voltage value of the voltage source; and

a trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of a second transistor of the transistor network,

wherein the transistor network comprises a first nFET and a second nFET connected in series with one another between the voltage source and a ground,

wherein the transistor network further comprises a third nFET connected in series with the first nFET and the second nFET between the voltage source and the ground, and

wherein the bias network further comprises a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor and a gate of the third nFET.

5. (Original) The power clamp of claim 1, wherein the bias network comprises a voltage divider configured to communicate a portion of the voltage from the voltage source to the gate of the first transistor.

6. (Original) The power clamp of claim 1, wherein the trigger network comprises a resistor and a capacitor configured to filter out non-electrostatic discharge events from the gate of the second transistor.

7. (Currently amended) A power clamp for an integrated circuit, comprising:

at least an upper and a lower nFET respectively connected in series with one

another between a pair of power supply rails from a higher potential to a lower potential;

a voltage divider configured to bias a gate of the upper nFET to a prescribed value; and

a low frequency filter connected to a gate of the lower nFET and configured to filter out low frequency signals between at least one power supply rail and the gate of the lower nFET.

8. (Original) The power clamp of claim 7, wherein the gate of the upper nFET is biased to a prescribed fraction of a voltage between the pair of power supply rails.

9. (Previously presented) The power clamp of claim 7, wherein the voltage divider is connected between the pair of power supply rails and comprises at least one bias network.

10. (Original) The power clamp of claim 9, wherein the voltage divider comprises at least one resistor.

11. (Original) The power clamp of claim 7, wherein the low frequency filter communicates with a source and a drain of the lower nFET.

12. (Currently amended) A method of protecting against electrostatic discharge, comprising:

configuring a gate of at least one upper transistor of a transistor network

connected between power rails to be biased to a prescribed value; and

coupling an electrostatic discharge event to a gate of a lower transistor of the transistor network,

wherein the at least one upper and at least one lower transistors of the transistor network are respectively coupled between the power rails from a higher voltage to a lower voltage.

13. (Original) The method of claim 12, further comprising biasing the gate of the at least one upper transistor with a voltage divider connected between the power rails.

14. (Previously presented) The method of claim 12, further comprising configuring the voltage divider to comprise at least one bias network.

15. (Original) The method of claim 14, further comprising biasing the gate of the at least one upper transistor to a prescribed fraction of the voltage of at least one power rail of the power rails.

16. (Original) The method of claim 12, wherein configuring a gate of at least one upper transistor of a transistor network connected between power rails to be biased to a prescribed value comprises applying a voltage to at least one power rail of the power rails.

17. (Original) The method of claim 12, wherein configuring a gate of at least

one upper transistor of a transistor network connected between power rails to be biased to a prescribed value comprises attaching a bias network between at least one power rail of the power rails and the transistor network.

18. (Original) The method of claim 12, further comprising coupling an electrostatic discharge event to a gate of a lower transistor with a high pass filter.

19. (Original) The method of claim 18, further comprising configuring the high pass filter to comprise a time constant of about one microsecond.

20. (Original) The method of claim 12, further comprising configuring at least one power rail of the power rails to be in electrical communication with a voltage source, and configuring at least one power rail of the power rails to be in electrical communication with ground.

AMENDMENT TO DRAWINGS

The sheet of drawings attached as part of the Appendix includes a New Sheet presenting new Figure 3a. The New Sheet addresses the Examiner's formal objection in the instant Office Action.

REMARKS

Upon entry of the instant amendment, the specification and claims 1, 7, and 12 will have been amended, and new Figure 3a will have been entered for consideration by the Examiner. Accordingly, claims 1 – 20 will remain pending in the application.

Summary of the Official Action

In the instant Office Action, the Examiner has withdrawn the indication of allowability of claim 4, objected to the drawings and claim 8, rejected claims 7 and 10 based upon formal matters, and rejected claims 1 – 20 over the art of record. By the present amendment and remarks, Applicants submit that the objections and rejections have been overcome, and respectfully request reconsideration of the outstanding Office Action and allowance of the present application.

Objection to Drawings is Moot

Applicants submit that the objection to the drawings for failure to show each recited feature of the invention is moot in view of the submission of the New Sheet illustrating new Figure 3a. Applicants note that, as this Figure shows the features recited in claims 3 and 4, the objection to the drawings is now moot. Further, Applicants note that the claims 3 and 4, as well as paragraph [0040] provide support for the subject matter shown in the new figure.

Accordingly, Applicants request that the Examiner reconsider and withdraw the objection to the drawings and indicate that the drawings are acceptable in the next official communication.

Traversal of Objection to the Claims

Applicants traverse the objection to claim 8 as being of improper dependent form

under 37 C.F.R. 1.75(c). Applicants note that claim 8 recites subject matter that further defines the "prescribed value" to which the gate of the upper nFET is biased, i.e., a prescribed fraction of a voltage between the pair of power supply rails.

Accordingly, as claim 8 further defines independent claim 7, Applicants submit that this claim is fully in compliance with the Patent Office Rules, and request that the Examiner reconsider and withdraw this objection.

Traversal of Rejection Under 35 U.S.C. § 112, First Paragraph

Applicants traverse the rejection of claims 7 and 10 under 35 U.S.C. § 112, first paragraph, as being indefinite.

Applicants note that, as the Examiner has only identified features of independent claim 7 in the rejection, it is believed that claim 10 was inadvertently included. Acknowledgement that claim 10 is not rejected is respectfully requested.

Moreover, Applicants note that it appears the Examiner is incorrectly construing the recited term "low frequency filter" as a low-pass filter, which it is not. Applicants' independent claim 7 clearly and unambiguously recites that the low frequency filter is configured to "filter out low frequency signal," which corresponds to the disclosure in paragraph [0031] of a "high pass filter."

Accordingly, Applicants request that the Examiner reconsider and withdraw the rejection of claim 7 (and 10) under 35 U.S.C. § 112, first paragraph, and indicate that the claims are fully in compliance with the requirements of the statute.

Traversal of Rejection Under 35 U.S.C. § 102(b)

Applicants traverse the rejection of claims 1, 2, 5, and 6 under 35 U.S.C. § 102(b) as being anticipated by ANDRESEN et al. (U.S. Patent No. 6,147,538)

[hereinafter "ANDRESEN"]. The Examiner asserts that Figure 8 of ANDRESEN shows all the recited features of the rejected claims. Applicants traverse the Examiner 's assertions.

Applicants' independent claim 1, as currently amended, recites, *inter alia*, a transistor network *composed of a first and second transistor respectively connected between a voltage source and a ground*, a *bias network configured to bias a gate of the first transistor* of the transistor network to a portion of a voltage value of the voltage source, and a *trigger network configured to communicate the occurrence of an electrostatic discharge event to the gate of the second transistor* of the transistor network. Applicants submit that ANDRESEN fails to disclose at least the above-noted features of the invention.

Applicants note that Figure 8 of ANDRESEN shows a series arrangement of transistors N1a and N1b respectively connected between a voltage source and ground. Thus, from this arrangement, transistor N1a would correspond to the recited first transistor and transistor N1b would correspond to the second transistor of independent claim 1.

Further review of Figure 8 reveals that the first N1a and second N1b transistors are biased to Vdd and approximately 0, respectively, and the first transistor N1a is triggered by control 804 in the event of an ESD zap. However, this arrangement is wholly inconsistent with the express recitation of at least independent claim 1, where a bias network is configured to bias a gate of the first transistor of the transistor network to a portion of a voltage value of the voltage source, and a trigger network is configured to communicate the occurrence of an electrostatic discharge event to the gate of the

second transistor of the transistor network.

Because the applied art fails to show each and every recited feature of at least independent claim 1, Applicants submit that ANDRESEN fails to provide an adequate evidentiary basis to support a rejection of anticipation under 35 U.S.C. § 102(b). Accordingly, Applicants request that the Examiner reconsider and withdraw this rejection.

Further, Applicants submit that claims 2, 5 and 6 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicants submit ANDRESEN fails to anticipate the features recited in claim 2, 5, and 6.

Accordingly, Applicants request the Examiner reconsider and withdraw the rejection of claims 1, 2, 5, and 6 under 35 U.S.C. § 102(b) and indicate these claims are allowable.

Traversal of Rejection Under 35 U.S.C. § 103(a)

1. *Over Andresen*

Applicants traverse the rejection of claims 3 and 4 under 35 U.S.C. § 103(a) as being unpatentable over ANDRESEN. The Examiner asserts that it would have been obvious to utilize additional transistors in gate coupled device 800 of ANDRESEN. Applicants traverse the Examiner's assertions.

In addition to the foregoing deficiencies of ANDRESEN, Applicants note that ANDRESEN fails to teach or suggest "swapping" the biasing of transistors N1a and N1b. Moreover, Applicants submit that, even assuming, *arguendo*, one ordinarily

skilled in the art were to find it obvious to switch the biasing of ANDRESEN, such that the first transistor is coupled to the junction between resistors R3a and R3b and the second transistor is coupled to control 804 (which Applicants submit one would not), the resulting modified system would no longer operate in the manner intended by its inventor.

That is, by switching the biasing of the transistors of gate coupled device 800 of ANDRESEN, such that the gate of first transistor N1a is connected to approximately 0 volts, the transistor switches would no longer operate in a manner to remove the ESD current, as intended by ANDRESEN.

Because ANDRESEN would not operated in its intended manner if modified in a manner that corresponds to the pending claims, Applicants submit that modification would not have been obvious, such that ANDRESEN fails to render unpatentable the instant invention recited in at least independent claim 1.

Further, Applicants submit that, contrary to the Examiner's assertions, ANDRESEN fails to teach or suggest that it would have been obvious to utilize another transistor in series with transistors N1a and N1b in gate controlled device 800. Moreover, as the gates of the transistors of device 800 of ANDRESEN are coupled to the uppermost and approximately the lowermost voltages, it is not apparent from ANDRESEN to what level one would obvious bias an additional series transistor without preventing the intended operation of ANDRESEN.

Further, Applicants submit that claims 3 and 4 are allowable at least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular,

Applicants submit ANDRESEN fails to anticipate the features recited in claim 3 and 4.

Accordingly, Applicants request the Examiner reconsider and withdraw the rejection of claims 3 and 4 under 35 U.S.C. § 103(a) and indicate these claims are allowable.

2. *Over Andresen in view of Lin*

Applicants traverse the rejection of claims 7 – 18 and 20 under 35 U.S.C. § 103(a) as being unpatentable over ANDRESEN in view of LIN et al. (U.S. Patent No. 6,919,602) [hereinafter "LIN"]. The Examiner acknowledges that ANDRESEN fails to teach or suggest clamp transistors and the RC filter being connected to the power supply rail, but that it would have been obvious to do so in view of LIN. Applicants traverse the Examiner's assertions.

Applicants' independent claim 7, as currently amended, recites, *inter alia*, at least *an upper and a lower nFET respectively connected in series with one another between a pair of power supply rails from a higher potential to a lower potential*, a voltage divider configured *to bias a gate of the upper nFET* to a prescribed value, and a *low frequency filter connected to a gate of the lower nFET and configured to filter out low frequency signals between at least one power supply rail and the gate of the lower nFET*. Further, Applicants' independent claim 12, as currently amended, recites, *inter alia*, configuring a gate of at least one upper transistor of a transistor network connected between power rails to be biased to a prescribed value, and *coupling an electrostatic discharge event to a gate of a lower transistor* of the transistor network, such that *the at least one upper and at least one lower transistors of the transistor network are respectively coupled between the power rails from a higher voltage to a lower voltage*. Applicants submit

that no proper combination of ANDRESEN and LIN renders unpatentable at least the above-noted features of the invention.

As discussed above, Figure 8 of ANDRESEN shows a series arrangement of transistors N1a and N1b respectively connected between a higher potential and a lower potential. Thus, from this arrangement, transistor N1a would correspond to the recited upper nFET (upper transistor) and transistor N1b would correspond to the lower nFET (lower transistor) of independent claim 7 (independent claim 12).

Moreover, Applicants have pointed out that Figure 8 also shows the upper nFET (transistor) N1a and lower nFET (transistor)N1b are biased to Vdd and approximately 0, respectively, and the upper nFET (transistor)N1a is triggered by control 804 in the event of an ESD zap. However, like the arrangement recited in Applicants' independent claim 1, this arrangement, too, is wholly inconsistent with the express recitation of at least independent claim 7, where a voltage divider configured to bias a gate of the upper nFET to a prescribed value, and a low frequency filter connected to a gate of the lower nFET and configured to filter out low frequency signals between at least one power supply rail and the gate of the lower nFET. Moreover, this arrangement is wholly inconsistent with the express recitation of at least independent claim 12, which includes configuring a gate of at least one upper transistor of a transistor network connected between power rails to be biased to a prescribed value, and coupling an electrostatic discharge event to a gate of a lower transistor of the transistor network.

As discussed above, ANDRESEN fails to teach or suggest "swapping" the biasing of transistors N1a and N1b, nor is there any suggestion that, if one were to switch the biasing of the transistors of device 800 of ANDRESEN, such that the first

transistor is coupled to the junction between resistors R3a and R3b and the second transistor is coupled to control 804, the resulting modified system would operate in the manner intended by its inventor.

Moreover, notwithstanding any features assertedly taught by LIN, Applicants note that LIN fails to teach or suggest the subject matter noted above as deficient in ANDRESEN, i.e., LIN also fails to teach or suggest the expressly recited arrangement of at least independent claims 7 and 12.

Because neither applied document teaches or suggests at least the above-noted features of at least independent claims 7 and 12, Applicants submit that no proper combination of these documents can even arguably render unpatentable the invention recited in these claims. Thus, Applicants submit that the asserted rejections are improper and should be withdrawn.

Further, Applicants note that LIN fails to provide any teaching or suggestion for modifying ANDRESEN in any manner that would render the present invention obvious. In fact, because Applicants have shown that modifying ANDRESEN in a manner to correspond to the recited features of at least independent claims 7 and 12 renders ANDRESEN inoperable for its intended purpose, Applicants submit that the art of record (including LIN) fails to suggest the requisite motivation or rationale for combining ANDRESEN and LIN in any manner that would even arguably render unpatentable the combination of features recited in at least independent claims 7 and 12.

Accordingly, reconsideration and withdrawal of the rejections of at least independent claims 7 and 12 is respectfully requested.

Further, Applicants submit that claims 8 – 11, 13 – 18 and 20 are allowable at

least for the reason that these claims depend from allowable base claims and because these claims recite additional features that further define the present invention. In particular, Applicants submit ANDRESEN fails to anticipate the features recited in claim 8 – 11, 13 – 18 and 20.

Accordingly, Applicants request the Examiner reconsider and withdraw the rejection of claims 7 – 18 and 20 under 35 U.S.C. § 103(a) and indicate these claims are allowable.

3. *Over Andresen*

Applicants traverse the rejection of claim 19 under 35 U.S.C. § 103(a) as being unpatentable over ANDRESEN. The Examiner asserts that it would have been obvious to set a time constant of the filter to one microsecond. Applicants traverse the Examiner's assertions.

Applicants note that, on its face, this rejection is improper and should be withdrawn. That is, as claim 19 depends from claim 18, which was rejected over an asserted combination of ANDRESEN and LIN, rejecting claim 19 over ANDRESEN alone is improper. Accordingly, reconsideration and withdrawal of this rejection is respectfully requested.

Moreover, Applicants have shown that ANDRESEN, whether alone or in any proper combination with LIN (or any other document of record), fails to render obvious the combination of features recited in at least independent claim 12.

Further, Applicants submit that claim 19 is allowable at least for the reason that it depends from an allowable base claim and because it recites additional features that further define the present invention. In particular, Applicants submit ANDRESEN fails

to anticipate the features recited in claim 19.

Accordingly, Applicants request the Examiner reconsider and withdraw the rejection of claim 19 under 35 U.S.C. § 103(a) and indicate these claims are allowable.

Application is Allowable

Thus, Applicants respectfully submit that each and every pending claim of the present invention meets the requirements for patentability under 35 U.S.C. §§ 102 and 103, and respectfully request the Examiner to indicate allowance of each and every pending claim of the present invention.

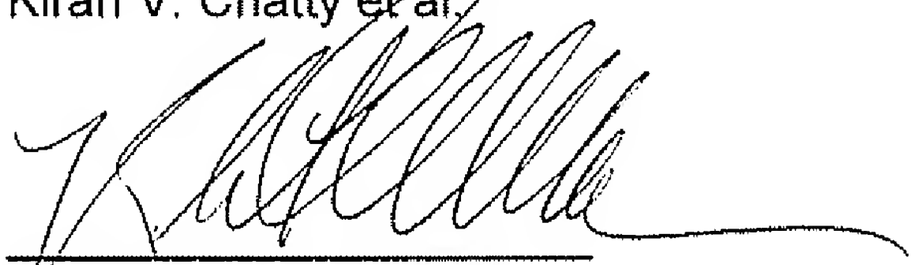
CONCLUSION

In view of the foregoing, it is submitted that none of the references of record, either taken alone or in any proper combination thereof, anticipate or render obvious the Applicants' invention, as recited in each of claims 1 – 20. The claims have been amended to eliminate any arguable basis for rejection under 35 U.S.C. § 112. In addition, the applied references of record have been discussed and distinguished, while significant claimed features of the present invention have been pointed out.

Further, any amendments to the claims which have been made in this response and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Accordingly, reconsideration of the outstanding Office Action and allowance of the present application and all the claims therein are respectfully requested and now believed to be appropriate.

Respectfully submitted,
Kiran V. Chatty et al.



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